REMARKS

Claims 1-47 are pending in the present application.

In the office action mailed March 24, 2006 (the "Office Action"), the Examiner rejected claims 1, 6, 7, 11, 14, 17-19, 24, 27, 28, 33, 37-41, and 43-47 were under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,324,485 to Ellis (the "Ellis patent"). The Examiner further rejected claims 4, 5, 12, 13, 20, 25-27, 29, 34-36, and 42 under 35 U.S.C. 103(a) as being unpatentable over the Ellis patent. The Examiner further commented on the number of references cited in information disclosure statements ("IDSs") and objected to the specification.

Information disclosure statements were submitted on February 13, 2004 and March 15, 2006. Applicant requests the Examiner consider the references cited in each Form PTO-1449 of the Information Disclosure Statements and provide the attorney of record with a signed and initialed copy of each Form PTO-1449.

The Examiner has suggested various duties of the Applicant with reference to the submission of material in an IDS. For example, the Examiner states that Applicant has a duty of making disclosure in such a way as not to "bury" pertinent prior art references within other disclosures of less relevant prior art. *See* the Office Action at page 2. Additionally, the Examiner states that Applicant has the duty to particularly point out any highly relevant material amongst the reference cited in an IDS. *See id.*

Applicant has not attempted to "bury" pertinent prior art with less relevant references in its submission of IDSs in the present application, and takes issue at the Examiner's suggestion that this may be the case. The references cited in the IDSs have been cited by Examiners in patent applications directed to subject matter related to the subject matter of the present patent application. The references have been cited in the present application out of an abundance of caution given the severe consequences of finding inequitable conduct by failing to cite relevant references. Moreover, the Applicant's various "duties" set forth by the Examiner do not appear to be substantiated by the code, case law, the rules, or the MPEP at this time. For example, the Examiner fails to cite support for the proposition that "it is the [A]pplicant's duty to particularly point out any highly relevance [sic] material amongst the references cited in the

IDS." *See* the Office Action at page 2. It is requested that the Examiner provide citation to authority that supports the proposition being made.

The Examiner has objected to the specification based on "numerous patent applications cited but not included in the references cited on the prior art 1449s submitted by the Applicant now given as related applications in the specification section 'Cross-References to Related Applications.'" *See* the Office Action at page 3. Applicant requests clarification of the Examiner's objection since cross-references to co-pending applications referenced in previously submitted IDSs have not been added to the specification of the present application.

Claims 1, 7, 19, and 28 have been amended to clarify the subject matter recited by the respective claim. It will be apparent from the amendments, and the remarks below, that the amendments were made independent of the references cited by the Examiner. None of previously mentioned amendments narrow or further limit the scope of the invention as recited by the respective claim. Consequently, the amendments should not be construed as being "narrowing amendments," because these amendments were not made for a substantial reason related to patentability.

Before discussing the rejection of the pending claims, embodiments of the invention will now be discussed in comparison to the applied references in order to help the Examiner appreciate certain distinctions between the pending claims and the subject matter of the applied references. Specific distinctions between the pending claims and the references will be discussed after the discussion of the disclosed embodiment and the references. This discussion of the differences between the disclosed embodiment and the applied references does not define the scope or interpretation of any of the claims.

The present invention includes an embodiment of a memory hub having a bypass path on which memory request packets are captured by the memory hub and forwarded to downstream memory hubs on downstream memory modules. As described in the present application, having the memory request packet bypass path allows the memory request packets to propagate to downstream memory modules. The bypass path of the memory hub is clocked according to a first clock signal having a first clock frequency. That is, the memory request packets are captured by the memory hub and transmitted to downstream memory modules at the first clock frequency. In contrast, local hub circuitry included in the memory hub, such as a

memory controller, operates according to a second clock signal having a second clock frequency. The second clock frequency is typically lower than the first clock frequency. By having the bypass path operating at the first clock frequency and having the local hub circuitry operating at the second slower clock frequency, the memory request packets can be propagated to the downstream memory modules at the faster clock frequency but processing of the memory request packets can still be at the slower clock frequency. Consequently, the logic circuits of the local hub circuitry can be simplified compared to designing higher speed local hub circuitry that operate at the first clock frequency. Additionally, delays in forwarding the memory request packets downstream can be minimized.

In the particular embodiment of the invention shown in Figure 3, capture registers 300 and 302 and capture FIFOs 304, 306 are clocked by MRCLK and MRCLK* signals, respectively, to capture the memory request packets in the high-speed link clock domain. The MRCLK and MRCLK* signals represent clock signals in the clock domain of the high-speed link. Capture registers 318, 320 also capture the memory request packets in the high-speed link clock domain by being clocked by the MTCLK and MTCLK* clock signals. The memory request packets are coupled to the capture registers 318, 320 over a bypass path 216. In contrast to the capture registers 300, 302, the capture registers 318, 320 are used to provide the memory request packets to downstream memory modules. As a memory request packet is coupled to the bypass path 216 and transmitted through the capture registers 318, 320 downstream to the next memory module in the high-speed link clock domain, a capture read pointer clocked by a CCLK signal selects which of the capture FIFOs 304, 306 provides a memory request packet to a memory controller 314. The CCLK signal represents a clock signal in the lock hub clock domain. As a result, the memory request packets are latched by the capture registers 300, 302, buffered in the FIFO buffers 304, 306, and transmitted to downstream memory modules by the capture registers 318, 320 at a faster rate of the high-speed link clock domain while the memory request packets are read out of the FIFO buffers 304, 306 under control of the read pointer circuit 308 and multiplexers 310, 312 at a slower rate of the local hub clock domain.

The Ellis patent is directed to a test system that attempts to simulate the native environment of a device under test ("DUT") in order to more accurately gauge the functionality and performance of the DUT. A native interface board that is designed to simulate the native

environment is driven by automated test equipment (ATE). The DUT is coupled to the native interface board during testing. For example, in one embodiment described in the Ellis patent for testing RAMBUS DRAM ("RDRAM") modules, the native interface board is represented by a PC motherboard 320 that uses RDRAM. The PC motherboard 320 is controlled by a ATE unit 340 during testing so that the PC motherboard 320 interacts with a RDRAM DUT 338 as it would in a native environment. The RDRAM DUT 338 is coupled to the PC motherboard 320 through a RAMBUS channel 332 to receive conventional RDRAM control signals.

A feature of the test systems described in the Ellis patent is the ability to control timing of the DUT relative to a system clock for the native interface board. A timing control module 315 is provided to provide the DUT with a clock signal having a controllable phase relative to a resident clock signal of the native interface board. In this manner, the clock-to-data time relationship at the DUT can be altered relative to the resident clock signal, which allows the tolerance or failure range of the DUT to be evaluated. The adjustable clock signal can be generated from the resident clock signal, or by using a separate substitute clock.

As previously discussed, claims 1, 6, 7, 11, 14, 17-19, 24, 27, 28, 33, 37-41, and 43-47 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Ellis patent.

Claims 1, 7, 14, 19, 28, 37, and 43 are patentably distinct from the Ellis patent because the Ellis patent fails to disclose the combination of limitations recited by the respective claim.

For example, with reference to claim 1, the Ellis patent fails to disclose the reception interface and the transmission interface as recited. The Examiner argues that the reception and transmission interfaces are disclosed by the "memory controller which both receives and transmits data and which provides various clock signals for testing memory modules by receiving and transmitting data based on different timing signals," citing col. 8, line 28-col. 10, line 40. *See* the Office Action at page 4. The material cited by the Examiner describes the embodiments of the test system illustrated in Figures 4 and 5A. As previously discussed, the test system described in the Ellis patent includes a substitute clock circuit that is used to generate a clock signal for the DUT. In the embodiment related to Figure 4 the substitute clock circuit is included on the RIMM riser card 410 to which the RDRAM DUT is connected. The RIMM riser card 410 is connected to the native interface board 402, which as previously

discussed, is used to closely simulate the native environment in which the RDRAM DUT will operate. The microprocessor 404, memory control hub 406 on the native interface board 402 are driven by a resident clock signal generated by the resident clock 405. The resident clock signal is also provided to the RIMM socket 408 to be provided to the RIMM riser card 410 along with TEST signals. The substitute clock signal generated by the timing control module 412 for the RDRAM DUT can be adjusted relative to the timing of the resident clock signal so that various timing margin of the RDRAM DUT can be evaluated.

As previously discussed, the Examiner has analogized the memory controller, which is assumed to be the memory control hub 406, to the reception and transmission interfaces recited in claim 1. Based on the description in the Ellis patent, the memory control hub 406 operates in accordance with the resident clock 405. Consequently, data is received and provided by the memory control hub 406 according to the same clock. In contrast, as recited in claim 1, the reception interface receives and captures data words in response to a first clock signal in a first time domain and provides groups of data words in response to a second clock signal in a second time domain. More generally, all of the circuitry on the native interface board described in the Ellis patent operates in accordance with the resident clock 405. That is, both the microprocessor 404 and the memory control hub 406 operate in accordance with one clock signal, namely, the resident clock signal. Thus, data that is captured by and transmitted from the native interface board is in accordance with one clock signal and not two different clock signals. Using the single resident clock 405 for the circuitry of the native interface board 402 is consistent with the feature of adjusting the clock signal clocking the DUT to evaluate timing margin. Receiving data words by the memory control hub 406 and providing the captured data words using two different clock signals introduces issues with which one of the different clock signals the timing of the substitute clock signal should be based. Moreover, with respect to the transmission interface as recited in claim 1, data words are received from the reception interface and captured in accordance with a third clock signal that is in the first time domain. The memory control hub 406, or the microprocessor 404, are not described in the Ellis patent as operating in accordance with a third clock signal that is in the same clock domain as the resident clock 405.

The material cited by the Examiner further describes the embodiment of the test system illustrated in Figure 5A. The particular test system is designed for testing a RDRAM RIMM DUT 508 coupled to a test environment having a memory controller and resident RDRAM RIMMs 504, 506. The DATA and ADDRESS/CONTROL signals are provided to all of the RDRAM RIMMs 504, 506, 508. Resident clock signals in the form of CTM/CFM signals are provided only to the resident RDRAM RIMMs 504, 506. The CTM/CFM clock signals are generated by a resident clock 514. The RDRAM RIMM DUT 508, however, is clocked by substitute CTM/CFM signals generated by a timing control circuit 516. As with the other embodiments of the test system described in the Ellis patent, the test system illustrated in Figure 5A allows for adjustment of the substitute CTM/CFM clock signals clocking the RDRAM RIMM DUT 508 relative to the CTM/CFM signals generated by resident clock 514 so that timing margin can be evaluated.

As with the embodiment illustrated in Figure 4, the memory controller 502, which the Examiner argues is analogous to the reception and transmission interfaces recited in claim 1, operates in accordance with the CTM/CFM clock signals generated by the resident clock 514. As shown in Figure 5A and described by the related material at col. 9, line 17-col. 10, line 40, the DATA and ADDRESS/CONTROL signals are provided to the RDRAM RIMMs 504, 506, and the RDRAM RIMM DUT 508 according to the CTM/CFM clock signals from the resident clock 514. Consequently, the memory controller 502 is not analogous to the reception interface recited in claim 1, which receives and captures data words in response to a first clock signal in a first time domain and provides groups of the captured data words in response to the second clock signal in a second time domain. As for the transmission interface, the memory controller 502 is not described as operating as recited in claim 1, or including circuitry similar to the transmission interface that receives data words from the reception interface and captures the same according to a third clock signal in the first time domain.

Claims 7, 19, and 28 include reception and transmission interface limitations similar to those previously discussed with respect to claim 1. As with claim 1, the Ellis patent fails to disclose the combination of limitations recited in claims 7, 19, and 28.

Claim 14 is also patentably distinct from the Ellis patent. The Ellis patent fails to disclose the combination of limitations recited by claim 14. For example, the Ellis patent fails to

disclose a memory hub having a bypass path as recited in claim 14. The Examiner has argued that the bypass path is analogous to "the test circuitry being separate from the RIMM sockets 1 and 3 of Figure 9." *See* the Office Action at page 5. Reviewing Figure 9 and the related description in the Ellis patent, it is uncertain how the test circuitry represents a "bypass path" as recited in claim 14. RIMM socket 1 904 represents a "known good" RDRAM RIMM and RIMM socket 3 908 represents a "C-RIMM" that provides continuity and termination for the RIMM signals transmitted by the memory controller 902. The test RIMM socket 906 is for coupling a timing riser card 910 that is used to test multiple RDRAM RIMM DUTs. Thus, rather than testing individual RDRAM devices or individual RDRAM RIMMs, the timing riser card 910 allows for several RDRAM RIMMs to be tested using a common substitute clock signal that is applied for all RIMMs coupled to the timing riser card 910.

The timing riser card 910 does not represent a bypass path because the data words provided to the timing riser card 910 are not coupled to any other circuitry other than those located on the timing riser card 910. That is, the path on which data words are provided to the timing riser card 910 does not circumvent any other circuitry but ends on the timing riser card 910. As shown in Figure 9, and described in the Ellis patent, "[d]ata signals 920 are terminated on the timing riser card [910] in data termination circuit 918, and are not routed back to the native interface board of the ATE system." *See* col. 13, lines 18-20. By failing to disclose a bypass path, the Ellis patent fails to anticipate the memory module as recited in claim 14.

Claims 37 and 43 are also patentably distinct from the Ellis patent because the Ellis patent fails to disclose the combination of limitations recited by the respective claim.

Claim 37 recites a method of processing downstream memory requests that includes latching received data words in each memory hub of the memory system, responsive to a first clock signal in a first clock domain. Claim 43 recites a method of processing downstream memory requests that includes capturing downstream data words in each memory hub in a first clock domain; bypassing each memory hub to provide each captured downstream data word to a next adjacent downstream memory hub; and processing in each memory hub the captured data word in a second clock domain being defined by clock signals having frequencies less than the frequencies of clock signals in the first clock domain.

The Examiner argues that the methods of claims 37 and 43 are anticipated by operation of the memory controller previously discussed with reference to claims 1, 7, 19, and 28. However, as shown in Figure 5A and described in the related text, not all of the memory modules of the test system are responsive a first clock signal in a first clock domain. As previously discussed, embodiments of the test system described in the Ellis patent allow for substitute clock signals clocking a RDRAM RIMM DUT to be adjusted relative to a resident clock signal that clocks all of the other RDRAM RIMMs in the test system. Consequently, the RDRAM RIMM DUT latches or captures data responsive to a different clock signal from the other RDRAM RIMMs in the test system. As recited in claim 37, received data words are latched by *each* memory hub of the memory system responsive to a first clock signal in a first clock domain, and as recited in claim 43, downstream data words in *each* memory hub are captured in a first clock domain.

For the foregoing reasons, claims 1, 7, 14, 19, 28, 37, and 43 are patentably distinct from the Ellis patent. Claim 6, which depends from claim 1, claim 11, which depends from claim 7, claims 17 and 18, which depend from claim 14, claims 24 and 27, which depend from claim 19, claim 33, which depends from claim 28, claims 38-41, which depend from claim 37, and claims 44-47, which depend from claim 43, are similarly patentably distinct based on their dependency from a respective allowable base claim. Therefore, the rejection of claims 1, 6, 7, 11, 14, 17-19, 24, 27, 28, 33, 37-41, and 43-47 under 35 U.S.C. 102(b) should be withdrawn.

As previously mentioned, claims 4, 5, 12, 13, 20, 25-27, 29, 34-36, and 42 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Ellis patent.

The Examiner has indicated that the Ellis patent "does not specifically teach the reception interface and transmission interface further comprises optical interface circuitry corresponding to the data words and converting the received optical signals into corresponding electrical signals or the transmitted data words for electrical signals for optical signals." *See* the Office Action at page 6. The Examiner has taken official notice that conversion of optical signals to electrical signals and vice versa, and the technology is old in the memory arts. *See id.* Applicant disagrees that the subject matter indicated by the Examiner is well-known, or is common knowledge in the art capable of instant and unquestionable demonstration as being well-known. Consequently, it is improper for the Examiner to take official notice of that matter.

If the Examiner maintains the rejection, Applicant requests that the Examiner provide documentary evidence of the facts asserted as well-known and common knowledge in the art.

Even if the Examiner's official notice is considered accurate, for the sake of argument, it fails to make up for the deficiencies of the Ellis patent previously discussed with reference to the rejections under 35 U.S.C. 102(b). As a result, the combined teachings of the Ellis patent and common knowledge in the art fails to teach or suggest the combination of limitations recited by claims 4, 5, 12, 13, 20, 25-27, 29, 34-36, and 42. Therefore, the rejection of these claims under 35 U.S.C. 103(a) should be withdrawn.

All of the claims pending in the present application are in condition for allowance. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

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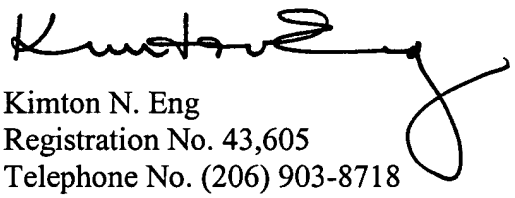

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